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H1R RAD R10 R17
U1S S1839

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EP 0186550 A2

(58) Field of search
UK CL (Edition K) B5N, H1R RAD
INT CL[5] B32B 18/00, H05K 3/46
Online databases: WPI

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(54) Ceramic three dimensional electronic structures

(57) A three dimensional integrated electronic structure include at least one substrate formed from a laminated stack of ceramic green unfired sheets, at least one of which has a printed circuit formed on its surface. The laminated stack is sintered and electronic devices are mounted on the sintered substrate. The substrate is shaped, formed, moulded or designed so as to provide thereto a predetermined profile suitable for mounting, fixing or locating the structure in a pre-selected enclosure apparatus, machine or the like. The predetermined profile can be given to the structure at any one of three stages in the production process thereof; viz a) before the laminating step; b) during the laminating step, and c) after the laminating step.

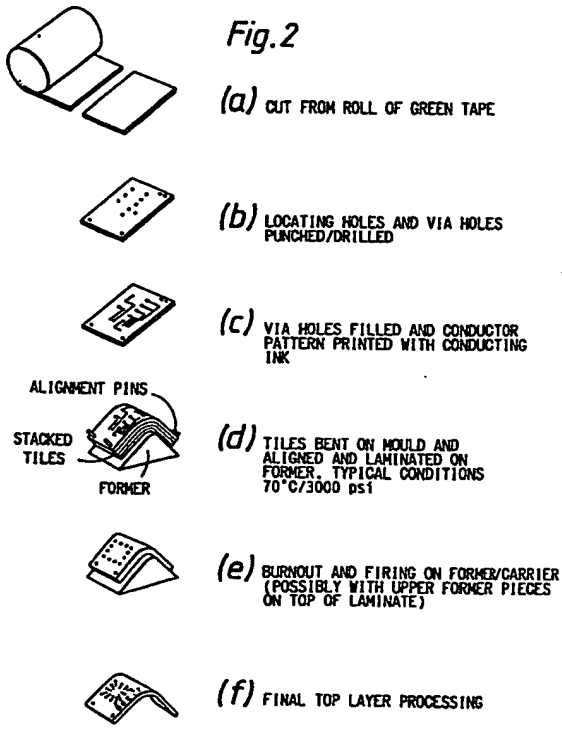
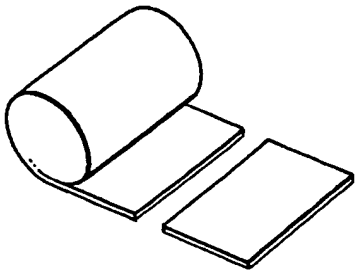


Fig.2

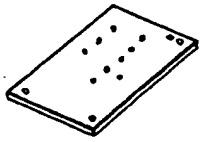
GB 2 255 451 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

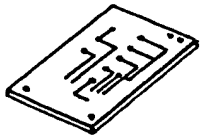
Fig.1



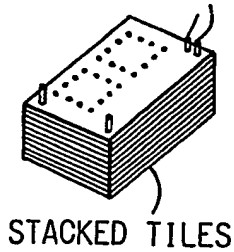
(a) CUT FROM ROLL OF GREEN TAPE



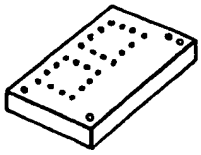
(b) LOCATING HOLES AND VIA HOLES PUNCHED/DRILLED



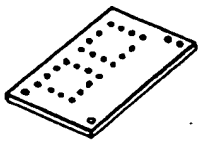
(c) VIA HOLES FILLED AND CONDUCTOR PATTERN PRINTED WITH CONDUCTING INK



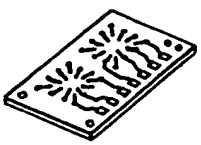
(d) ALIGNED AND LAMINATED TYPICAL CONDITIONS 70°C,3000 psi PRESS



(e) BURNOUT AT TYPICALLY 350°C/1HR.

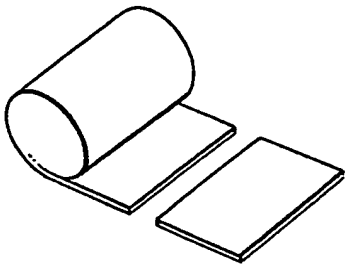


(f) FIRING AT 850°C PEAK

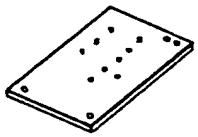


(g) FINAL TOP LAYER PROCESSING

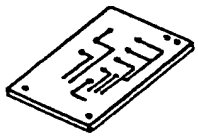
Fig. 2



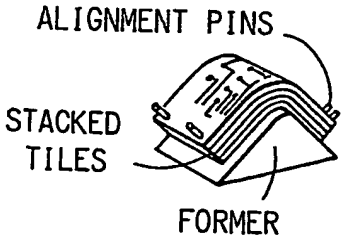
(a) CUT FROM ROLL OF GREEN TAPE



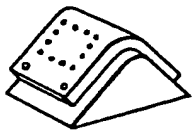
(b) LOCATING HOLES AND VIA HOLES PUNCHED/DRILLED



(c) VIA HOLES FILLED AND CONDUCTOR PATTERN PRINTED WITH CONDUCTING INK



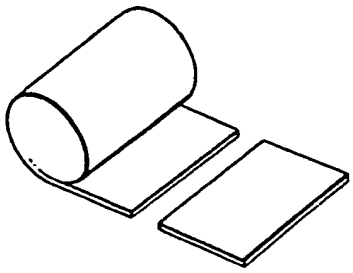
(d) TILES BENT ON MOULD AND ALIGNED AND LAMINATED ON FORMER. TYPICAL CONDITIONS 70°C/3000 psi



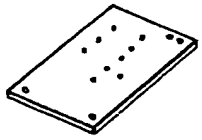
(e) BURNOUT AND FIRING ON FORMER/CARRIER (POSSIBLY WITH UPPER FORMER PIECES ON TOP OF LAMINATE)

(f) FINAL TOP LAYER PROCESSING

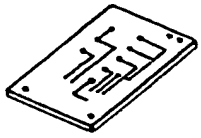
Fig.3



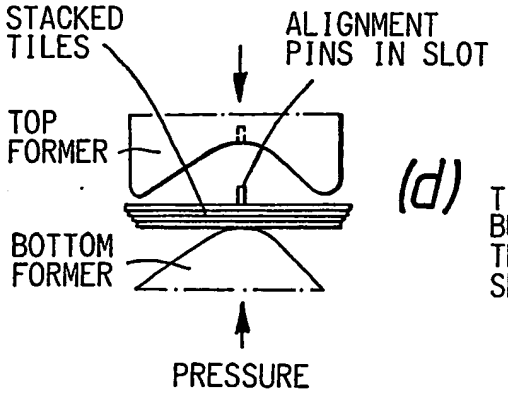
(a) CUT FROM ROLL OF GREEN TAPE



(b) LOCATING HOLES AND VIA HOLES PUNCHED/DRILLED



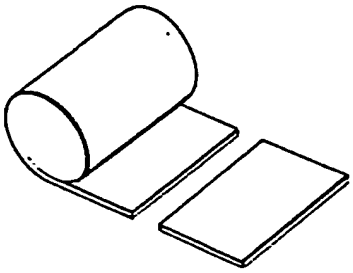
(c) VIA HOLES FILLED AND CONDUCTOR PATTERN PRINTED WITH CONDUCTING INK



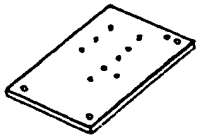
PLAN VIEW

(d) TILES ALIGNED IN FLAT STACK, BUT LAMINATED AT MODERATE TEMPERATURE + PRESSURE OVER SHAPED FORMER

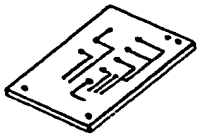
Fig. 4



(a) CUT FROM ROLL OF GREEN TAPE



(b) LOCATING HOLES AND VIA HOLES PUNCHED/DRILLED



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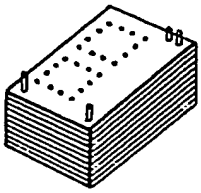
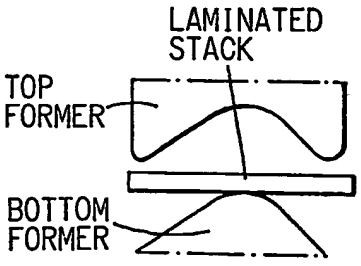


(d) TILES STACKED, ALIGNED AND COMPACTED



PLAN VIEW

(e) FLAT STACK PLACED ON SHAPED FORMER OR MOULD AND BURNTOUT AND FIND AS BEFORE

Ceramic Three Dimensional Electronic Structures

This invention relates to monolithic three dimensional electronic structures and a method of making the same. The three dimensional electronic structures of the present invention will give military and professional electronic designers additional design freedoms to better utilise the space available to them, in a high reliability format. It utilises the newly developed low-dielectric, low-temperature firing, glass-ceramic tapes to make reliable, three dimensional substrates which combine the electrial interconnect function with that of structural support.

Demands for increased performance from aviation equipment has led to a proliferation in electronic sub-systems, all struggling to fit into a weight/volume envelope which is already under pressure from the performance requirements of the overall system. Silicon integration, and novel interconnection schemes such as multichip modules are helping to ease that pressure, but the finite size of passive components and the interconnection structures, coupled with the limited and often non-orthogonal spaces that sub-systems must be fitted into, mean increasing problems for the designer, not assisted by a constant customer demand for reduced costs and greater value for money. The introduction of more integrated opto-electronics into

these systems is likely to make the matter worse, with demands for minimum bend radii for lightguides and line of sight interconnections.

Similar pressures in the area of consumer electronics, assisted by the introduction of engineering polymers capable of withstanding soldering temperatures, has led to the development of three dimensional moulded printed circuit boards. These claim to offer better electrical and mechanical performance than standard pcbs; greater design freedom with the removal of the need to accomodate all the components on flat circuit boards; space savings by incorporating components onto the structure of the equipment; improved reliability by integrating connectors into the structure; and reduced costs, due to the elimination of the need to machine slots, recesses or vias in the board. Additional cost savings arise during the assembly process as it is possible to mould component holding fixtures, snap-ons and stiffening ribs into the initial basic structure. Over the last few years a large number of technologies and prototypes have been developed. The production of such structures has required a great deal of development of the infrastructure; in the design and development in 3-D CAD tools; methods of placing and holding components on non-planar surfaces; soldering methods; test and inspection. Not all of these problems have been solved but progress has been made and some products, usually with an integrated electrical/mechanical function, have been produced.

In the military and professional environment, apart from some early proposals for electronic integration into the composite skin of an aircraft (a concept now known as 'smart skin'), little work is known in the field of structural/electronic integration. Three dimensional structures are used but are built up by hand from individual flat substrates. An example of this approach is the Tx/Rx unit, which is used in large numbers in some phase array radars. These have a distributor circuit mounted on the lens at the base of the structure, with the Tx unit fixed vertically on one side of it and the Rx circuit on the other side to form a 'U' shaped unit. Electrical connection, and some of the mechanical strength, is

achieved through hand made solder joints where the units meet. This results in units that are costly to build, with unit to unit variability due to the hand soldered joint.

According to the invention there is provided a three dimensional integrated electronic structure including a substrate or substrates, the substrate or each substrate being formed of a laminated stack of ceramic green sheets, at least one of the ceramic green sheets of the substrate or each substrate having a printed circuit formed on the surface thereof, said laminated stack of green sheets or each of said laminated stack of green sheets being sintered and electronic devices mounted on said sintered substrate or substrates and wherein said substrate or each said substrate is shaped, formed, moulded or designed so as to provide thereto a predetermined profile suitable for mounting, fixing or locating said structure in a preselected enclosure, apparatus, machine or the like.

According to one embodiment of a method of forming the three dimensional electronic structure of the present invention, each of said green ceramic sheets is shaped, formed, moulded or designed such that when said sheets are laminated and sintered, said structure of predetermined profile is formed.

According to another embodiment of a method of forming the three dimensional electronic structure of the present invention, the stack of sheets or each of said stack of sheets is shaped, formed, moulded or designed during lamination thereof to provide said predetermined profile thereto.

According to still another embodiment of a method of forming the three dimensional electronic structure of the present invention, said laminated stack of green sheets is shaped, formed, moulded or designed during sintering thereof to provide said predetermined profile thereto.

The stack of green sheets or each said stack of green sheets may be laminated at a temperature of 60°C to 150°C and at a pressure between 3.45×10^3kPa and 3.45×10^4kPa (500 Psi and 5000 Psi) using

copper or graphite formers for example to achieve said predetermined profile.

Typically the stacks of green sheets are laminated at a temperature of 70°C and a pressure of 2.1×10^4kPa (3000 Psi).

The invention will now be described further by way of example with reference to the accompanying drawings in which:

Figure 1a-g illustrates a conventional method of forming a known two dimensional integrated electronic structure;

Figure 2a-f illustrates a method of forming a three dimensional integrated electronic structure embodying the present invention;

Figure 3a-d illustrates another method of forming a three dimensional integrated electronic structure embodying the present invention;

Figure 4a-e illustrates an alternative method of forming a three dimensional integrated electronic structure embodying the present invention.

The advent of low temperature firing ceramic tapes in 'green' (ie unfired) form could allow an opportunity for military systems to gain some of the benefits of moulded circuit boards combined with the benefits and reliability of cofired and thick film technology. These materials are a mixture of ceramic powders with suitable binders and are supplied unfired in the form of rolls of unfired tape (Fig. 1a). The production sequence for conventional flat substrates, well known to those skilled in the art, is shown in outline in Fig. 1a to Fig. 1g and is described in more detail by J.I.Steinberg, S. J. Horowitz & R. J. Bacher, in "Low Temperature Co-Fired Dielectric Material System for Multi-Layer Interconnections", 5th European ISHM Conference, Stresa, Italy, May 1985. The process starts by cutting tiles from the roll of tape (Fig. 1a). The tile is then punched with a series of small via holes, to allow later interconnection through the substrate, along with larger holes for alignment pins (Fig. 1h). The via holes are then filed with a conducting paste or ink, and a pattern of conductors

is printed on the surface of the tile in the same or compatible ink system (Fig. 1c). The tile and inks are then allowed to dry before it is stacked with other tiles on alignment pins and subjected to moderate heat and pressure, of the order of 70°C and 2.1×10^4kPa (3000 psi) (Fig. 1d). Final burn out is carried out in two steps. The laminated substrate is placed on a flat carrier and burnt out in air, typically at 350°C for one hour (Fig. 1e), removing about 85% of the organic materials in this process. The same carrier and tile is then passed, in a one hour cycle, through a standard thick film firing oven with with a peak temperature of 850°C for 15 minutes. The tile now has the final dimension (Fig. 1f). The final processes, printing and firing the surface conductors and trimming any resistors etc, are now carried out (Fig 1g) to produce a flat, co-fired, application specific ceramic (or more correctly glass-ceramic) substrate. Recent developments in low temperature ceramic tape technology have produced material of lower dielectric constant (5.8) than alumina and claimed insertion losses of 0.2 dB/inch at 10GHz, (twice that at 20GHz), making the substrate potentially useful at microwave frequencies.

This invention consists of a method of modifying the process used in making these flat co-fired ceramic substrates to produce shaped substrates. In addition, inserts, cut-outs and recesses could be cut in the green material before the stack is laminated, complete with any additional stand-offs and component locations . Different design rules would be needed from those applied to standard, flat structures made from low-temperature firing tape, to allow for the relative movement between the planes, differential shrinkage and geometric restrictions on shrinkage.

These modifications can take place at three stages in the production process; before the laminating step; during the laminating step; or after this stage. Figures 2a-f show the steps needed for the pre-laminating shaping process, where the tiles are bent whilst still in the unfired, green stage. At this stage the tape has the consistency of hard rubber and can be bent into non-planar shapes, possibly using a former or mould (Fig. 2d).

Assemblies of these 'bent' sheets could be assembled on a former, using alignment pins in slits to allow for the shrinkage on firing, and laminated into 'bent' substrates (Figs 2d to 2f). Figures 3a-d show the process of moulding the shaped substrate from a flat stack of tiles during the lamination stage, using the moderate temperatures and pressures to push the stack onto a shaped former. The final method illustrated in Figures 4a-4e does not use applied pressure on the laminated flat stack, but relies on the lack of structural strength of the substrate during burn-out and firing to enable the pliable substrate to take up the shape of the former it is sitting on.

In all three methods described with reference to Figures 2 to 4, the shaped laminated substrate would then be cofired, populated with devices and soldered. The final structure should show improved mechanical and electrical reliability due to the removal of the soldered joints, improved electrical performance both from the improved dielectric properties of the materials and from the reduced reflections from smooth, rounded transitions in board direction; better space utilizations and improved value for money due to savings on assembly.

CLAIMS

1. A three dimensional integrated electronic structure including a substrate or substrates, the substrate or each substrate being formed of a laminated stack of ceramic green sheets, at least one of the ceramic green sheets of the substrate or each substrate having a printed circuit formed on the surface thereof, said laminated stack of green sheets or each of said laminated stack of green sheets being sintered and electronic devices mounted on said sintered substrate or substrates and wherein said substrate or each said substrate is shaped, formed, moulded or designed so as to provide thereto a predetermined profile suitable for mounting, fixing or locating said structure in a preselected enclosure, apparatus, machine or the like.

2. A method for forming a three dimensional integrated electronic structure as claimed in Claim 1, in which each of said green ceramic sheets is shaped, formed, moulded or designed such that, when said sheets are laminated and sintered, said structure of predetermined profile is formed.

3. A method of forming a three dimensional integrated electronic structure as claimed in Claim 1, in which said stack of sheets or each said stack of sheets is shaped, formed, moulded or designed during lamination thereof to provide said predetermined profile thereto.

4. A method of forming a three dimensional integrated electronic structure as claimed in Claim 1, in which said laminated stack of green sheets or each said laminated stack of green sheets is shaped, formed, moulded or designed during sintering thereof to provide said predetermined profile thereto.

5. A method as claimed in Claim 3, in which said stack of green sheets or each said stack of green sheets is laminated at a temperature of 50°C to 150°C and at a pressure between 3.45×10^3kPa and 3.45×10^4kPa (500 Psi and 5000 Psi) using copper or graphite formers to achieve said predetermined profile.

6. A method as claimed in Claim 5, in which said stack of green sheets or each said stack of green sheets is laminated at a temperature of 70°C and at a pressure of 2.1×10^4kPa (3000 Psi).

7. A three dimensional integrated electronic substrate/structure substantially as hereinbefore described with reference to any one of figures 2 to 4 of the accompanying drawings.

8. A method of forming a three dimensional electronic structure substantially as hereinbefore described with reference to figures 2 to 4 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
9109687.5

Relevant Technical fields

(i) UK Cl (Edition K) H1R (RAD); B5N

(ii) Int Cl (Edition 5) H05K 3/46; B32B 18/00

Search Examiner
P CORBETT

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES : WPI

Date of Search
19.09.91

Documents considered relevant following a search in respect of claims 1 TO 8

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	EP 0186550 A2 FUJITSU - see lines 3-20, page 5	1

Category	Identity of document and relevant passages	Relevant to claim(s)

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A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

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